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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10072934	FILING DATE 02/12/2002	CLASS 327.11	SUBCLASS 15.1	GAU 2188 2616	EXAMINER Braddon
**APPLICANTS: Matsuo Yoshikatsu;					
**CONTINUING DATA VERIFIED: None RVD					
**FOREIGN APPLICATIONS VERIFIED: ex RVD JAPAN 2001-35559 02/13/2001					
PG-PUB <input type="checkbox"/>		DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>	
Foreign priority claimer: <input checked="" type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 conditions met: <input checked="" type="checkbox"/> yes <input type="checkbox"/> no				ATTORNEY DOCKET NO F00ED362	
Verified and Acknowledged Examiners's initials <i>elo</i>					
TITLE : Memory control circuit				U.S. DEPT. OF COMM. #PAT & TM PTO 4361 (Rev. 12-94)	

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg. Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner	
		Application Examiner	
		PREPARED FOR ISSUE	
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